Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of the claims in the application:

What is claimed is:

1. (Previously Presented) A multi-layer integrated semiconductor structure, comprising:

(a) a first device layer having first and second opposing surfaces, said first device layer including:

a first substrate having a first surface corresponding to the first surface of the first device layer and having a second opposing surface, the first substrate having provided therein a first plurality of doped regions which form at least part of one or more semiconductor elements;

a dielectric material having first and second opposing surfaces with the first dielectric material surface disposed over the second surface of the first substrate and wherein the second surface of the dielectric material corresponds to the second surface of the first device layer; and

a first conductive via provided in the dielectric material, the first conductive via having a first end electrically coupled to at least one of the first plurality of doped regions and a second end exposed through the second one of the first and second surfaces of the dielectric material;

(b) a conductive interface having a first surface and a second opposing surface with the first surface of the conductive interface disposed over at least a portion of the second surface of the dielectric material such that at least a portion of the conductive interface is coupled to at least a portion of the first end of the first conductive via in the first device layer;

(c) a second device layer having first and second opposing surfaces, with the first surface of said second device layer disposed over the second surface of the conductive interface, the second device layer including:

a second substrate having first and second opposing surfaces and having provided therein a second plurality of doped regions which form at least part of one or more semiconductor elements;

an insulating material having a first surface disposed against the second opposing surface of the conductive interface and a second opposing surface of the insulating material disposed against a first one of the first and second opposing surfaces of the second substrate and wherein the second device layer is secured to the first device layer via the conductive interface; and

a second conductive via provided in the second device layer, said second conductive via having a first end directly coupled to the conductive interface and having a second end coupled to at least one of the second plurality of doped regions such that an electrical communication path between the first device layer and the second device layer is provided by the first conductive via, the conductive interface and the second conductive via.

2. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1 further comprising a first conductive interconnect element disposed in the dielectric material of the first device layer with a first end of the first conductive interconnect element coupled to the first conductive via and a second end of the first conductive interconnect element coupled to at least one of the first plurality of doped semiconductor elements.

3. (Cancelled)

4. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1 further comprising a second conductive interconnect having a first portion disposed over at least a portion of one of the second plurality of doped regions and having a second portion coupled to the second end of the second conductive via.

5. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1, further comprising a second conductive interconnect disposed in the second device layer and coupled to the second conductive via provided in the second device layer.

6. (Previously Presented) The multi-layer integrated semiconductor structure of claim 5, wherein the second conductive interconnect is coupled to at least one of the one or more semiconductor elements of the second device layer.

7. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1, wherein the second conductive via includes a first end coupled to the at least one of the one or more semiconductor elements in the second device layer and a second end coupled to the first conductive interface.

8. (Previously Presented) The multi-layer integrated semiconductor structure of claim 7, wherein the second device layer comprises a second conductive interconnect having a first portion coupled to the second conductive via and a second portion coupled to at least one element of the second plurality of semiconductor elements such that the second conductive interconnect couples the second conductive via to the at least one element of the second plurality of semiconductor elements..

9. (Cancelled)

10. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1 further comprising a third conductive via provided in the first device layer, wherein the third conductive via is coupled between a portion of the first conductive interconnect and the at least one of the first plurality of doped regions.

11. (Previously Presented) The multi-layer integrated semiconductor structure of claim 10 further comprising a second conductive interface disposed over a first surface of the second device layer and wherein the second conductive via forms at least a part of an electrical communication path between the second conductive interconnect and at least a portion of the second interface.

12. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1, wherein the first conductive via forms at least a portion of a signal path between the conductive interface and at least one of the first and second plurality of semiconductor elements.

13. (Previously Presented) The multi-layer integrated semiconductor structure of claim 12, wherein the second end of the first conductive via is coupled to the at least one element of the

first plurality of semiconductor elements.

14. (Previously Presented) The multi-layer integrated semiconductor structure of claim 1, wherein the first conductive interface comprises copper.

15. (Previously Presented) The multi-layer integrated semiconductor structure of claim 14 wherein the conductive interface is provided as a first conductive interface region and the multi-layer integrated semiconductor structure further comprises a second conductive interface region disposed between the first and second device layers with the second conductive interface region being physically separated from the first conductive interface region.

16. (Previously Presented) The multi-layer integrated semiconductor structure of claim 15, wherein the second interface region includes an adhesive material such that the second interface region secures the first device layer to the second device layer.

17. (Previously Presented) A multi-layer integrated semiconductor structure, comprising:

(a) at least a first device layer having first and second opposing surfaces, said first device layer including:

a first substrate having a first surface corresponding to the first surface of the first device layer and having a second opposing surface, the first substrate having provided therein at least a first doped semiconductor region which forms at least part of one or more semiconductor elements; and

a first dielectric material having first and second opposing surfaces with the first dielectric material surface disposed about the first doped semiconductor region and wherein the second surface of the first dielectric material corresponds to the second surface of the first device layer, said dielectric material having at least a first via-hole with a first conductive material disposed therein to provide a first conductive via having first and second opposing ends with a first one of the first and second ends of the first conductive via electrically coupled to a at least a portion of at least one of the one or more semiconductor elements and a second one of the first and second ends of the first conductive via exposed through the second surface of the first dielectric material; and

(b) at least a second device layer having first and second opposing surfaces, with the first surface of said second device layer including:

a second substrate having first and second opposing surfaces and having provided therein at least a second doped semiconductor region which forms at least part of one or more semiconductor elements; and

a second dielectric material having first and second opposing surfaces with the first dielectric material surface disposed about the second doped semiconductor region and the second surface of the second dielectric material corresponding to the second surface of the second device layer and wherein said second substrate includes a second via-hole having a second conductive material disposed therein to provide a second conductive via having first and second ends with a first one of the first and second ends of the second conductive via electrically coupled to at least a portion of at least one of the one or more semiconductor elements of the second substrate and a second one of the first and second ends of the second conductive via is exposed through the second surface of the second dielectric material; and

(c) a first conductive interface having a first surface and a second opposing surface with the first surface of the conductive interface disposed between at least a portion of a first one of the first and second opposing surfaces of the first device layer and at least a portion of a first one of the first and second opposing surfaces of the second device layers such that at least a portion of the first conductive interface secures together the first and second device layers and also electrically couples the first device layer to the second device layer wherein the conductive interface and the first and second conductive vias form at least a portion of an electrical communication path between the first device layer and the second device layer.

18. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17 further comprising a first conductive interconnect element disposed in the first device layer with a first portion of the first conductive via electrically coupled to at least a portion of the first conductive interconnect element and a second portion of the first conductive interconnect element coupled to the first doped semiconductor region.

19. (Previously Presented) The multi-layer integrated semiconductor structure of claim 18,

wherein the first conductive via couples the first conductive interconnect element to the first conductive interface.

20. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the second conductive via is formed on the first one of the first and second opposing surfaces of the second device layer and is coupled to the second doped semiconductor region.

21. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17 further comprising a third conductive via coupled to the second doped semiconductor region.

22. (Previously Presented) The multi-layer integrated semiconductor structure of claim 21 further comprising a second conductive interface disposed on the second one of the first and second opposing surfaces of the second device layer and wherein the third conductive via is provided having a first end coupled to the second doped semiconductor region and a second end coupled to the second conductive interface.

23. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the second conductive via is formed on the first one of the first and second opposing surfaces of the second device layer and wherein the second device layer further comprises a first conductive interconnect.

24. (Previously Presented) The multi-layer integrated semiconductor structure of claim 23, wherein the second conductive via is provided having a first end coupled to the first conductive interconnect and a second end coupled to the first conductive interface.

25. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the first conductive via is coupled to at least the first doped semiconductor region.

26. (Previously Presented) The multi-layer integrated semiconductor structure of claim 25, wherein the first conductive via is provided having a first end coupled to at least the first doped semiconductor region and a second end coupled to the first conductive interface.

27. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the first interface corresponds to a first conductor interface region and the multi-layer integrated semiconductor structure further comprises a second interface region disposed between the first one of the first and second device layers with the second interface region provided from a non-conductive material.

28. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the first conductive interface region is provided from a conductive bonding material.

29. (Previously Presented) The multi-layer integrated semiconductor structure of claim 18, further comprising a second conductive interconnect element disposed in the second device layer with a portion of the second conductive interconnect element coupled to the second conductive via and wherein the first conductive via, the first conductive interface and the second conductive via provide a direct vertical electrical connection between the first conductive interconnect element and the second conductive interconnect element.

30. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer is constructed and arranged to operate using at least one of electronic components, optical components or micro-electromechanical components.

31. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer is constructed and arranged to operate using at least one of electronic components, optical components or micro-electromechanical components.

32. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes at least one die element.

33. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer includes at least one die element.

34. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes at least one die element of a plurality of die elements located on a semiconductor wafer.

35. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the second device layer includes at least one die element of a plurality of die elements located on a semiconductor wafer.

36. (Original) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area whereby the first predetermined surface area differs from the second predetermined surface area.

37. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer includes a first predetermined surface area and the second device layer includes a second predetermined surface area which is substantially equivalent to the first predetermined surface area.

38. (Previously Presented) The multi-layer integrated semiconductor structure of claim 17, wherein the first device layer further comprises:

a first conductive interconnect element having a first portion coupled to the first doped semiconductor region, and a second portion coupled to a first end of the first conductive via.

39. (Previously Presented) The multi-layer integrated semiconductor structure of claim 38, wherein the second device further comprises a second conductive interconnect element having a first portion coupled to the second doped semiconductor region and a second portion coupled to a first end of the second conductive via with the second end of the first conductive via and the second end of the second conductive via each coupled to the first interface.

40. (Previously Presented) A multi-layer semiconductor structure, comprising:

a first semiconductor wafer having first and second opposing surfaces, said first

semiconductor wafer including a first plurality of semiconductor structures each of which includes a first plurality of semiconductor elements, said first semiconductor wafer also comprising a first plurality of conductive vias, at least some of said first plurality of conductive vias disposed such that a first end of thereof is electrically coupled to at least some of said first plurality of semiconductor elements and a second end is exposed through one of the first and second surfaces of the first semiconductor wafer;

a second semiconductor wafer having first and second opposing surfaces, said second semiconductor wafer including a second plurality of semiconductor structures each of which includes a second plurality of semiconductor elements, said second semiconductor wafer also comprising a second plurality of conductive vias, at least some of said second plurality of conductive vias disposed such that a first end of thereof is electrically coupled to at least some of said second plurality of semiconductor elements and a second end is exposed through one of the first and second surfaces of the second semiconductor wafer; and

at least a first conductive bonding interface segment disposed between a first one of the first and second opposing surfaces of the first semiconductor wafer and a first one of the first and second opposing surfaces of the second semiconductor wafer, said first conductive bonding interface segment disposed over at least a first one of the plurality of semiconductor structures of the first semiconductor wafer and being in an electrical communication relationship through the first plurality of conductive vias electrically coupled to the first plurality of semiconductor elements with at least a first one of the first plurality of the semiconductor elements of the first semiconductor structure and at least a first one of the plurality of semiconductor elements of the second semiconductor structure of the second semiconductor wafer where the first conductive bonding interface segment and at least some of the first and second plurality of conductive vias form electrical signal paths between at least some of the first semiconductor elements of the first semiconductor structure and at least some of the second semiconductor elements of the second semiconductor structure.

41. Cancelled.